Hardware support for Gfx Sharing and Safe Rendering

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Gfx sharing hardware features

- H/W compositor layers
  - IP that provides separate h/w display layers with composition and alpha functionality. E.g. R-Car H3 VSPDx IP
  - Safety OS writes to layer 1, IVI to layer 2 etc. Layer 2 can not overwrite layer 1.
- IPMMU (IOMMU)
  - Per IP MMU for memory protection / robustness.
  - Only pass permitted access requests, combined with target-side memory and I/O protection
  - May have additional features, e.g. OS ID
- General purpose safety features
  - RTOS orientated CPUs, e.g. Cortex R7 on R-Car H3. Lock-step processing etc.
- Acceleration IP
  - E.g. video compression for surface sharing
- Bus QoS
  - QoS Controller time slice bus master access to DDR based on QoS params.
  - Best effort or fixed bandwidth.
  - Prioritise data from high priority bus masters.
- H/W GPU virtualization
  - see separate presentation for details

- What will be in h/w next-gen?

Safe Rendering

- DISCOM (Display Compare Unit)
  - Sits between memory bus and DU
  - CRC checker that output is correct. Calculation area selectable.
- Display Output Checker
  - Sits between DU and display
  - Checks whether display content, e.g. Tell-tales, are correctly output by the DU
  - Multiple definable check areas
  - Need to avoid false alarms. Are CRC checkers alone sufficient?
  - Multiple features. Granular checking, e.g. partly obscured or dimmed output.
  - Active Monitor raises interrupt on failures
- Various general support functions
  - Watchdogs, ECC memory, FuSA options, etc.
- How far to go?
  - Run s/w on real time or general purpose CPU? R7 vs A57/A53.
  - Dedicated h/w rendering path?
    - R-Car provides option of dedicated 2D GPU
    - GPU, composition layers, IPMMU, DU

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